



COLLISION OUTPUTS ARE ACTIVE LOW (IDLE HIGH)

CAUTION! GATE 5 IS NOR BUT DRAWN AS NAND!

F & J WILL IDLE HIGH NOR SR LATCH INPUTS F & J MUST IDLE HIGH (BOTH LOW IS NOT ALLOWED)

NAND SR LATCH EXPECTS F & J TO IDLE LOW AND WILL NOT WORK. THIS IS DRAWN WRONG, GATE 5 MUST BE NOR

VIDEO BALL GAME (VIDEO SECTION)

IC1, 2, 3, 9, 10 : 74C00 IC4, 5, 6, 7, 8, 11, 12, 13 : 74C02
 TR1, 2 : BC548 TR3 : BC 558 TR4 : BF173
 ALL DIODES : 1N914, 1N4148